The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A circuit for use in a digital display unit of a computer system, and circuit for generating a plurality of pixel data elements from an analog image data received by said digital display unit, said digital display unit further receiving a time reference signal associated with said analog image data, said time reference signal having a high frequency, said circuit comprising:

an analog-to-digital converter (ADC) for receiving said analog image data, said ADC sampling said analog image data using a sampling clock to generate a plurality of pixel data elements corresponding to said plurality of pixels, wherein said sampling clock has a sampling frequency equal to said high frequency;

a clock generator circuit comprising a phase-locked loop (PLL) circuit for generating said sampling clock, wherein said sampling clock is synchronized with said time reference signal with a jitter of less than a few nano-seconds, said PLL comprising:

a discrete time oscillator (DTO) for receiving a digital input and generating a signal representative of said sampling clock with a frequency determined by said digital input; and

a digital circuit for receiving said time reference signal and a feedback signal, wherein said feedback signal is generated by dividing said sampling clock, said digital circuit generating said digital input according to the difference of the phases of said time reference signal and said feedback signal, said digital input causing said DTO to generate said signal synchronized with said time reference signal, said digital circuit comprising:

a frequency correction logic for adjusting the phase of said sampling clock according to the long-term drifts in the frequency of said time reference signal; and

a phase correction logic for adjusting the phase of said sampling clock according to the phase difference in said feedback signal and said time reference signal,

wherein said frequency correction logic and said phase correction logic are implemented as two separate control loops,

wherein a panel interface included in said digital display unit can generate display signals for a display screen based on said plurality of pixel data elements.

2. (original) The circuit of claim 1, wherein said clock generator circuit further comprises an analog filter to eliminate any undesirable frequencies from said signal representative of said sampling clock to generate said sampling clock.

3. (original) The circuit of claim 1, further comprising a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal.

4. (original) The circuit of claim 3, further comprising a charge/discharge control logic for determining the amount of phase correction to be made based on the determination of said difference of phase.

5. (original) The circuit of claim 1, wherein said analog image data and said time reference signal are received on two separate signal paths.

6. (original) The circuit of claim 5, wherein said reference clock comprises a binary signal.

7. (original) The circuit of claim 1, wherein said digital circuit distributes phase error between said feedback signal and said reference signal during a comparison cycle by changing the phase of individual clock pulses in said sampling clock.

8. (original) The circuit of claim 1, wherein said frequency correction logic generates a multi-bit number, wherein said multi-bit number is representative of the amount of phase advance of said sampling clock generated by said DTO during a DTO clock period, and wherein said multi-bit representation enables said PLL to reach said sampling frequency within a short duration.

9. (original) The circuit of claim 1, wherein said frequency correction logic comprises:

a first multiplexor accepting as input Pnom and Fdp values, wherein Pnom represents an expected frequency of said sampling clock and Fdp represents the correction due to the long-term frequency drifts;

a flip-flop for storing a value representative of the phase correction corresponding to the frequency correction logic;

an adder for adding or subtracting the output of said first multiplexor from the value stored in said flip-flop, wherein the output of said adder is stored in said flip-flop; and

a frequency correction control coupled to said flip-flop and said adder, wherein said frequency correction control causes said flip-flop to be set to Pnom at the beginning of a phase acquisition phase, and wherein said frequency correction control causes said adder to add or subtract Fdp depending on whether the sampling clock is early or late in comparison to said time reference.

10. (original) The circuit of claim 1, further comprising:

a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal, wherein said phase and frequency detector asserts an EARLY signal a number of clock pulses proportionate to the difference of phase by which said feedback signal is earlier than said time reference signal and a or a LATE signal a number of pulses proportionate to the difference of phase by which said feedback signal is later than said time reference signal; and

a charge/discharge control logic implemented using digital components, said charge/discharge control logic including a phase integrator, said charge/discharge control logic charging said phase integrator according to the number of pulses said EARLY signal or said LATE signal is asserted, said charge/discharge logic discharging over a longer period of time than the charging period so as to spread the difference in phase over a comparison cycle, wherein the phase of said sampling clock is corrected during the discharging period.

11. (original) The circuit of claim 10, further comprising a sign and zero crossing detector for correcting any over-correction performed by said charge/discharge logic during said discharging period.

12. (new)A circuit for use with a digital display unit for generating a plurality of digital image data elements from analog image data received by said digital display unit, wherein said digital display unit further receives a time reference signal having a time reference signal frequency associated with said analog image data, said circuit comprising:

an analog-to-digital converter (ADC) for sampling said analog image data using a sampling clock to generate said plurality of digital image data elements:

a clock generator circuit for generating said sampling clock that is synchronized with said time reference signal and that receives a digital input and generates a signal representative of said sampling clock with a frequency determined by said digital input; and

a digital circuit for receiving said time reference signal and a feedback signal, wherein said feedback signal is generated by dividing said sampling clock, said digital circuit generating said digital input according to the difference of the phases of said time reference signal and said feedback signal, said digital input causing said clock generator circuit to generate said signal synchronized with said time reference signal.

13. (new)The circuit of claim 12, wherein said clock generator circuit further comprises:

an analog filter to eliminate any undesirable frequencies from said signal representative of said sampling clock to generate said sampling clock; and

a phase-locked loop (PLL) circuit that includes a discrete time oscillator (DTO).

14. (new)The circuit of claim 12, further comprising a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal.

15. (new)The circuit of claim 14, further comprising a charge/discharge control logic for determining the amount of phase correction to be made based on the determination of said difference of phase.

16. (new)The circuit of claim 12, wherein said analog image data and said time reference signal are received on two separate signal paths.

17. (new)The circuit of claim 16, wherein said reference clock comprises a binary signal.

18. (new)The circuit as recited in claim 12, wherein said sampling clock has a sampling frequency equal to said time reference signal frequency.

19. (new)The circuit as recited in claim 12, further comprising:

a frequency correction logic for adjusting the phase of said sampling clock according to the long-term drifts in said time reference signal frequency; and

a phase correction logic for adjusting the phase of said sampling clock according to the phase difference in said feedback signal and said time reference signal,

wherein said frequency correction logic and said phase correction logic are implemented as two separate control loops.

20. (new)The circuit as recited in claim 12, wherein said digital display comprises:

a display screen; and

a panel interface arranged to generate display signals for the display screen based on said plurality of digital image data elements.

21. (new)The circuit of claim 19, wherein said digital circuit distributes phase error between said feedback signal and said reference signal during a comparison cycle by changing the phase of individual clock pulses in said sampling clock.

22. (new)The circuit of claim 19, wherein said frequency correction logic generates a multi-bit number, wherein said multi-bit number is representative of the amount of phase advance of said sampling clock generated by said DTO during a DTO clock period, and wherein said multi-bit representation enables said PLL to reach said sampling frequency within a short duration.

23. (new) The circuit of claim 19, wherein said frequency correction logic comprises:

a first multiplexor accepting as input Pnom and Fdp values, wherein Pnom represents an expected frequency of said sampling clock and Fdp represents the correction due to the long-term frequency drifts;

a flip-flop for storing a value representative of the phase correction corresponding to the frequency correction logic;

an adder for adding or subtracting the output of said first multiplexor from the value stored in said flip-flop, wherein the output of said adder is stored in said flip-flop; and

a frequency correction control coupled to said flip-flop and said adder, wherein said frequency correction control causes said flip-flop to be set to Pnom at the beginning of a phase acquisition phase, and wherein said frequency correction control causes said adder to add or subtract Fdp depending on whether the sampling clock is early or late in comparison to said time reference.

24. (new)The circuit of claim 12, further comprising:

a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal, wherein said phase and frequency detector asserts an EARLY signal a number of clock pulses proportionate to the difference of phase by which said feedback signal is earlier than said time reference signal and a or a LATE signal a number of pulses proportionate to the difference of phase by which said feedback signal is later than said time reference signal; and

a charge/discharge control logic implemented using digital components, said charge/discharge control logic including a phase integrator, said charge/discharge control logic charging said phase integrator according to the number of pulses said EARLY signal or said

LATE signal is asserted, said charge/discharge logic discharging over a longer period of time than the charging period so as to spread the difference in phase over a comparison cycle, wherein the phase of said sampling clock is corrected during the discharging period.

25. (new)The circuit of claim 24, further comprising a sign and zero crossing detector for correcting any over-correction performed by said charge/discharge logic during said discharging period.

26. (new)A method of scaling a source image frame formed of a number of source image elements to provide a destination image frame formed of a number of destination image elements, comprising:

receiving said source image elements in accordance with a source frame rate;

scaling said source image elements independently in both vertical and horizontal directions to form said destination image elements; and

forming said destination image frame by providing said destination image elements in accordance with a destination frame rate, wherein said source frame rate is substantially equal to said destination frame rate.

27. (new)A method of claim 26, wherein a source image includes one or more of said source image frames, and wherein a destination image corresponding to said source image is generated by generating a destination image frame corresponding to each of said source image frames.

28. (new)A method as recited in claim 26, wherein when said scaling is upscaling, said scaling further comprises:

replicating a plurality of said source image elements to obtain replicated source image elements.

29. (new)A method as recited in claim 28, said scaling further comprising:

interpolating selected ones of said source image elements and said replicated source image elements to generate said destination image elements.

30. (new)A method as recited in claim 29, wherein said source image frame includes a plurality of source scan lines each of which includes a number of said source image elements, and wherein the destination image frame includes a plurality of destination scan lines each of which includes a number of said destination image elements.

31. (new)A method as recited in claim 30, further comprising:

using at least a present scan line and a previous scan line for said interpolation, wherein said present scan line and said previous scan line are included in said plurality of source scan lines.

32. (new)A method of claim 31, wherein at least one of said source scan lines is used one or more times as a present scan line.

33. (new)A method as recited in claim 26, wherein said source image frame has an associated source image frame aspect ratio and wherein said destination image frame has an associated destination image frame aspect ratio, wherein said scaled destination image frame aspect ratio is different from said source image frame aspect ratio.

34. (new)A method as recited in claim 26, wherein said source frame rate is based upon a first clock signal and wherein said destination frame rate is based upon a second clock signal.

35. (new)A method as recited in claim 34, further comprising:

storing said source image elements being received into a line buffer in accordance with said first clock signal; and

thereafter, outputting said destination image elements in accordance with said second clock signal.

36. (new)A method of claim 35, wherein said second clock signal is locked to said first clock signal in a proportion.

37. (new)A method of claim 36, wherein said proportion is equal to a ratio of a total number of source image elements to a total number of destination image elements.

38. (new)A digital display unit having a display screen for displaying a destination image frame formed of a number of destination image elements, comprising:

a display unit interface for displaying the destination image frame at a display rate based upon a display clock signal;

a converter circuit for generating a plurality of digital source image elements from an analog source image received by said digital display unit based upon a sampling clock signal wherein the analog source image has a associated time reference signal and time reference signal frequency;

a scaler unit coupled to the converter circuit arranged to

receive said digital source image elements in accordance with a first clock signal,

scale said source image elements independently in both vertical and horizontal directions to form said destination image elements, and

provide said destination image elements in accordance with a second clock signal to the display unit interface wherein the first clock signal and the second clock signal are arranged such that a source frame rate and a destination frame rate are substantially equal; and

a clock circuit arranged to produce the display clock signal, the sampling clock signal, the first clock signal and the second clock signal, wherein the sampling clock is synchronized with the time reference signal.

39. (new)A digital display unit as recited in claim 38, wherein the clock circuit receives a digital input and generates a signal representative of said sampling clock with a frequency determined by said digital input.

40. (new)A digital display unit as recited in claim 39, further comprising:

a digital circuit for receiving said time reference signal and a feedback signal, wherein said feedback signal is generated by dividing said sampling clock, said digital circuit generating said digital input according to the difference of the phases of said time reference signal and said feedback signal, said digital input causing said clock circuit to generate said sampling clock signal synchronized with said time reference signal.

41. (new)A method of displaying an analog source image by a digital display unit having a display screen as a destination image frame formed of a number of destination image elements wherein the analog source image has a associated time reference signal and time reference signal frequency, comprising:

synchronizing a sampling clock signal to the time reference signal;

generating a plurality of digital source image elements from said analog source image based upon said sampling clock signal;

optionally scaling said digital source image elements by a scaler unit by

receiving said digital source image elements at a source frame rate in accordance with a first clock signal, and

scaling said source image elements independently in both vertical and horizontal directions to form said destination image elements; and

providing said destination image elements at a destination frame rate in accordance with a second clock signal to the display unit interface, wherein said source frame rate is substantially equal to said destination frame rate; and

displaying the destination image elements by the digital display.

42. (new)A method as recited in claim 41, further comprising:

receiving a digital input that causes said clock circuit to generate said signal synchronized with said time reference signal; and

generating a signal representative of said sampling clock with a frequency determined by said digital input.

43. (new)A method as recited in claim 42, comprising:

generating a feedback signal by dividing said sampling clock; and

receiving said time reference signal and a feedback signal, wherein the digital input is based upon the difference of the phases of said time reference signal and said feedback signal.

44. (new) A memory efficient display controller for upscaling a source image at a first resolution to a destination image at a second resolution, comprising:

an interface arranged to receive source image pixel data in accordance with a first clock;

a line buffer having a size in accordance with a first resolution scan line length arranged to receive the source image pixel data at a second clock and store the received source image pixel data therein; and

an interpolator coupled to the line buffer arranged to form the destination image using selected stored source image pixel data read from said line buffer in accordance with the second clock.

45. (new) A display controller as recited in claim 44, wherein said interpolator comprises:

a vertical interpolator unit arranged convert a first resolution number of scan lines to a second resolution number of scan lines; and

a horizontal interpolator unit coupled to the vertical interpolator unit arranged to convert each of the second resolution number of scan lines each having the first resolution scan line length to a second resolution scan line length.

46. (new) A display controller as recited in claim 45, wherein the interpolator further comprises:

a second line buffer coupled to the vertical interpolator and the line buffer for storing only a previous scan line.

47. (new) A display controller as recited in claim 46, further comprising:

a third line buffer for storing a current scan line used with the previous scan line by the vertical interpolator to convert the first resolution number of scan lines to the second resolution number of scan lines.

48. (new) A display controller as recited in claim 45, wherein the line buffer is a single port memory type line buffer or wherein the line buffer is a dual ported memory type line buffer.

49. (new) A display controller as recited in claim 48, wherein when the line buffer is the single port SDRAM, then the line buffer further comprises a first bank and a second bank each having a size in accordance with the first resolution scan line length.

50. (new) A display controller as recited in claim 49, wherein when pixel data corresponding to a source image scan line is received in the first bank, then pixel data corresponding to another source image scan line can be concurrently read from the second bank as many times as required.

51. (new) A display controller as recited in claim 48, wherein when said line buffer comprises the dual-ported memory, the data is read from a port that is different from a port that receives the source image pixel data.

52. (new) A display controller as recited in claim 44, wherein the second clock is locked to said first clock in a proportion.

53. (new) A display controller as recited in claim 52, wherein the proportion is equal to (Htotal.sub.-- src.times.Vtotal.sub.-- src)/(Htotal.sub.-- dst.times.Vtotal.sub.-- dst), wherein Htotal.sub.-- src and Htotal.sub.-- dst represent the total number of pixels in each source scan line and each destination scan line respectively, and Vtotal.sub.-- src and Vtotal.sub.-- dst represent the total number of lines in the source image and the destination image, respectively.

54. (new) The display controller of claim 53, wherein the source image pixel data is received using an externally generated first clock that is locked to said first clock.

55. (new) The display controller of claim 44, wherein said source image has a source image aspect ratio and said destination image has a destination image aspect ratio that can be not equal to said source aspect ratio.

56. (new) The display controller of claim 44, wherein when said source image is an analog source image then the first clock is provided to a sampling circuit coupled to the interface that samples the analog source image at a sampling frequency such that each scan line in said source image is sampled a number of times equal to a number of pixels in each scan line in the destination image.

57. (new) A display controller as recited in claim 44, wherein an overrun condition in the line buffer is avoided by commencing writing the source image pixel data in a particular portion of the line buffer after the reading of the stored pixel data has commenced in that same portion of the line buffer.

58. (new) A display controller as recited in claim 44 further comprising:

an incomplete interpolated scan line suppressor unit coupled to the interpolator unit arranged to suppress a last incomplete scan line after the horizontal interpolation based upon a truncated vertical scaling factor (VSF).

59. (new) A display controller as recited in claim 58, wherein the truncated VSF is derived by truncating a fractional portion of VSF where VSF is equal to the ratio Vsize.sub.--src/Vsize.sub.—dst.

60. (new) The display controller of claim 44, wherein said display controller is coupled to a display unit.

61. (new) A display controller as recited in claim 60, wherein said display unit comprises an fixed array monitor selected from a group comprising: an LCD monitor and a plasma monitor.

62. (new) A display controller as recited in claim 61, wherein display unit is part of a television system.

63. (new) A display controller as recited in claim 44, wherein the first resolution corresponds to VGA and wherein the second resolution corresponds to a resolution selected from a group comprising: XGA, SXGA, UXGA, WQSXGA, and QSXGA.

64. (new) A display controller as recited in claim 44, wherein the display controller is formed as a single integrated circuit.

65. (new) A memory efficient method for upscaling a source image at a first resolution to a destination image at a second resolution, comprising:

receiving source image pixel data in accordance with a first clock;

receiving the source image pixel data a line buffer having a size in accordance with the first resolution at a second clock;

storing the received source image pixel data in the line buffer;

reading selected stored image pixel data from the line buffer at the second clock; and

forming the destination image using the selected stored source image pixel data.

66. (new) A method as recited in claim 65, wherein the forming the destination image comprises:

converting a first resolution number of scan lines to a second resolution number of scan lines; and

converting each of the second resolution number of scan lines each having a first resolution scan line length to a second resolution scan line length.

67. (new) A method as recited in claim 66, wherein the converting the first resolution number of scan lines to the second resolution number of scan line is based upon using a current scan line and a previous scan line.

68. (new) A method as recited in claim 65, wherein the line buffer is a single port memory type line buffer or wherein the line buffer is a dual ported memory type line buffer.

69. (new) A method as recited in claim 68, wherein when the line buffer is the single port SDRAM, then the line buffer further comprises a first bank and a second bank each having a size in accordance with the first resolution scan line length.

70. (new) A method as recited in claim 69, wherein when pixel data corresponding to a source image scan line is received in the first bank, then pixel data corresponding to another source image scan line can be concurrently read from the second bank as many times as required.

71. (new) A method as recited in claim 68, wherein when said line buffer comprises the dual-ported memory, the data is read from a port that is different from a port that receives the source image pixel data.

72. (new) A method as recited in claim 65, further comprising:

locking the second clock to the first clock in a proportion.

73. (new) A method as recited in claim 72, wherein the proportion is equal to (Htotal.sub.-- src.times.Vtotal.sub.-- src)/(Htotal.sub.-- dst.times.Vtotal.sub.-- dst), wherein Htotal.sub.-- src and Htotal.sub.-- dst represent the total number of pixels in each source scan line and each destination scan line respectively, and Vtotal.sub.-- src and Vtotal.sub.-- dst represent the total number of lines in the source image and the destination image, respectively.

74. (new) A method as recited in claim 65, wherein the source image pixel data is received using an externally generated first clock.

75. (new) A method as recited in claim 65, wherein said source image has a source image aspect ratio and said destination image has a destination image aspect ratio that can be not equal to said source aspect ratio.

76. (new) A method as recited in claim 65, wherein when said source image is an analog source image then the first clock is provided to a sampling circuit coupled to the interface that samples the analog source image at a sampling frequency such that each scan line in said source image is sampled a number of times equal to a number of pixels in each scan line in the destination image.

77. (new) A method as recited in claim 65, further comprising:

commencing writing the source image pixel data in a particular portion of the line buffer after the reading of the stored pixel data has commenced in that same portion of the line buffer thereby avoiding an overrun condition in the line buffer.

78. (new) A method as recited in claim 66 further comprising:

suppressing a last incomplete scan line based upon a truncated vertical scaling factor (VSF).

79. (new) A method as recited in claim 78, wherein the truncated VSF is derived by truncating a fractional portion of VSF where VSF is equal to the ratio Vsize.sub.--src/Vsize.sub.—dst.

80. (new) A method as recited in claim 65, wherein said display controller is coupled to a display unit.

81. (new) A method as recited in claim 80, wherein the display unit comprises an fixed array monitor selected from a group comprising: an LCD monitor and a plasma monitor.

82. (new) A method as recited in claim 81, wherein the display unit is part of a television system.

83. (new) A method as recited in claim 65, wherein the first resolution corresponds to VGA and wherein the second resolution corresponds to a resolution selected from a group comprising: XGA, SXGA, UXGA, WQSXGA, and QSXGA.

84. (new) A method as recited in claim 65, wherein the display controller is formed as a single integrated circuit.

85. (new) Computer program product for memory efficient upscaling of a source image at a first resolution to a destination image at a second resolution, comprising:

computer code for receiving source image pixel data in accordance with a first clock;

computer code for receiving the source image pixel data a line buffer having a size in accordance with the first resolution at a second clock;

computer code for storing the received source image pixel data in the line buffer;

computer code for reading selected stored image pixel data from the line buffer at the second clock;

computer code for forming the destination image using the selected stored source image pixel data; and

computer readable medium for storing the computer code.

86. (new) Computer program product as recited in claim 85, wherein the forming the destination image comprises:

computer code for converting a first resolution number of scan lines to a second resolution number of scan lines; and

computer code for converting each of the second resolution number of scan lines each having a first resolution scan line length to a second resolution scan line length.

87. (new) Computer program product as recited in claim 86, wherein the converting the first resolution number of scan lines to the second resolution number of scan line is based upon using a current scan line and a previous scan line.

88. (new) Computer program product as recited in claim 85, wherein the line buffer is a single port memory type line buffer or wherein the line buffer is a dual ported memory type line buffer.

89. (new) Computer program product as recited in claim 88, wherein when the line buffer is the single port SDRAM, then the line buffer further comprises a first bank and a second bank each having a size in accordance with the first resolution scan line length.

90. (new) Computer program product as recited in claim 89, wherein when pixel data corresponding to a source image scan line is received in the first bank, then pixel data corresponding to another source image scan line can be concurrently read from the second bank as many times as required.

91. (new) Computer program product as recited in claim 88, wherein when said line buffer comprises the dual-ported memory, the data is read from a port that is different from a port that receives the source image pixel data.

92. (new) Computer program product as recited in claim 85, further comprising: computer code for locking the second clock to the first clock in a proportion.

93. (new) Computer program product as recited in claim 92, wherein the proportion is equal to (Htotal.sub.-- src.times.Vtotal.sub.-- src)/(Htotal.sub.-- dst.times.Vtotal.sub.-- dst), wherein Htotal.sub.-- src and Htotal.sub.-- dst represent the total number of pixels in each source scan line and each destination scan line respectively, and Vtotal.sub.-- src and Vtotal.sub.-- dst represent the total number of lines in the source image and the destination image, respectively.

94. (new) Computer program product as recited in claim 85, wherein the source image pixel data is received using an externally generated first clock.

95. (new) Computer program product as recited in claim 85, wherein said source image has a source image aspect ratio and said destination image has a destination image aspect ratio that can be not equal to said source aspect ratio.

96. (new) Computer program product as recited in claim 85, wherein when said source image is an analog source image then the first clock is provided to a sampling circuit coupled to the interface that samples the analog source image at a sampling frequency such that each scan line in said source image is sampled a number of times equal to a number of pixels in each scan line in the destination image.

97. (new) Computer program product as recited in claim 85, further comprising:

computer code for commencing writing the source image pixel data in a particular portion of the line buffer after the reading of the stored pixel data has commenced in that same portion of the line buffer thereby avoiding an overrun condition in the line buffer.

98. (new) Computer program product as recited in claim 86 further comprising:

computer code for suppressing a last incomplete scan line based upon a truncated vertical scaling factor (VSF).

99. (new) Computer program product as recited in claim 98, wherein the truncated VSF is derived by truncating a fractional portion of VSF where VSF is equal to the ratio Vsize.sub.-- src/Vsize.sub.—dst.

100. (new) Computer program product as recited in claim 85, wherein said display controller is coupled to a display unit.

101. (new) Computer program product as recited in claim 100, wherein the display unit comprises an fixed array monitor selected from a group comprising: an LCD monitor and a plasma monitor.

102. (new) Computer program product as recited in claim 101, wherein the display unit is part of a television system.

103. (new) Computer program product as recited in claim 85, wherein the first resolution corresponds to VGA and wherein the second resolution corresponds to a resolution selected from a group comprising: XGA, SXGA, UXGA, WQSXGA, and QSXGA.

104. (new) Computer program product as recited in claim 85, wherein the display controller is formed as a single integrated circuit.